

What is claimed is:

1. An integrated circuit device comprising:
a conductive pad to receive an input signal from an external
signal line;
a first doped region, underlying and surrounding the
conductive pad;
a conductive region disposed in the first doped region;
a first tap region spaced apart from and surrounding a
substantial portion of the first doped region, wherein the first
tap region is electrically coupled to a first supply voltage;
an output driver transistor having a drain region and a source
region, wherein the drain region is electrically coupled to the
conductive pad; and
a second tap region surrounding the output driver transistor,
wherein the second tap region is electrically and physically
coupled to a second supply voltage and the source region.

2. The integrated circuit device of claim 1 wherein the
first and second supply voltages are ground.

3. The integrated circuit device of claim 2 wherein the
first tap region substantially surrounds the first doped region in
a concentric-like manner.

1 4. The integrated circuit device of claim 3 wherein the
2 first tap region is a discontinuous region.

1 5. The integrated circuit device of claim 1 wherein the
2 first doped region is of a first doping density of a first
3 conductivity type, the conductive region is of a second doping
4 density of the first conductivity type wherein the first doping
5 density is less than the second doping density.

1 6. The integrated circuit device of claim 1 wherein the
2 first tap region is a third doped region and the second tap region
3 is a fourth doped region.

1 7. The integrated circuit device of claim 1 wherein the
2 third doped region is of an opposite conductivity type than the
3 first doped region.

1 8. The integrated circuit device of claim 1 wherein the
2 fourth doped region is a P type doped region and the output driver
3 transistor is an NMOS type transistor.

1 9. The integrated circuit device of claim 1 wherein a
2 portion of the first tap region is decoupled from the first supply

3 voltage to provide a predetermined equivalent series resistance
4 between the first doped region and the first supply voltage.

1 10. The integrated circuit device of claim 1 wherein the
2 first tap region substantially surrounds the first doped region in
3 a concentric-like manner.

1 11. The integrated circuit device of claim 10 wherein the
2 first tap region is a discontinuous region.

1 12. A bond pad for an integrated circuit device, the bond pad
2 comprising:

3 a conductive bonding layer;

4 a first doped region, underlying and surrounding the
5 conductive bonding layer;

6 a conductive region disposed in the first doped region, the
7 conductive region having a surface area at least substantially
8 equal to the surface area of the conductive bonding layer; and

9 a conductive tap region spaced apart from and surrounding at
10 least a portion of the first doped region, wherein a portion of the
11 conductive tap region is electrically coupled to a supply voltage.

1 13. The bond pad of claim 12 wherein the supply voltage is a
2 ground voltage and the conductive bonding layer includes a metal.

1 14. The bond pad of claim 12 wherein the first doped region
2 is of a first doping density of a first conductivity type the
3 conductive region is of a second doping density of the first
4 conductivity type wherein the first doping density is less than the
5 second doping density.

1 15. The bond pad of claim 12 wherein the conductive tap
2 region is a third doped region and is of an opposite conductivity
3 type than the first doped region.

1 16. The bond pad of claim 12 wherein a portion of the
2 conductive tap region is decoupled from the supply voltage to
3 provide a predetermined equivalent series resistance between the
4 doped region and the supply voltage.

1 17. The bond pad of claim 12 wherein the conductive tap
2 region is a continuous region.

1 18. The bond pad of claim 17 wherein the conductive tap
2 region substantially surrounds the doped region in a concentric-
3 like manner.

1 19. The bond pad of claim 12 wherein the conductive tap
2 region is a discontinuous region.

1 20. The bond pad of claim 19 wherein the conductive tap
2 region substantially surrounds the doped region in a concentric-
3 like manner.

1 21. The bond pad of claim 12 wherein the conductive region is
2 polysilicon.

1 22. The bond pad of claim 21 wherein the conductive tap
2 region is an doped layer positioned beneath the conductive region.

1 23. A transistor layout for an integrated circuit device
2 having a bond pad, the transistor layout comprising:

3 a drain region electrically coupled to the bond pad;

4 a source region; and

5 a conductive tap region spaced proximal to and surrounding the
6 drain region, wherein the conductive tap region is electrically
7 coupled to a supply voltage and electrically and physically coupled
8 to the source region.

1 24. The transistor layout of claim 23 wherein the supply
2 voltage is coupled to a ground voltage.

1 *sub* 25. The transistor layout of claim 23 wherein the conductive
2 *com* tap region is an opposite conductivity type to a conductivity type
3 of the source region.

1 26. The transistor layout of claim 23 wherein the conductive
2 tap region is spaced proximal to and surrounds the drain region.

1 27. The transistor layout of claim 23 wherein the conductive
2 tap region is a discontinuous region.

1 28. The transistor layout of claim 23 further including:
2 a plurality of source regions, each source region of the
3 plurality of source regions being electrically and physically
4 coupled to the conductive tap region;

5 a plurality of drain regions, each drain region of the
6 plurality of drain regions being electrically coupled to the
7 bond pad; and

8 wherein the conductive tap region is spaced proximal to and
9 surrounds at least one drain region of the plurality of drain
10 regions.

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